ABSTRACT

The present invention provides a circuit to shift the level of an arbitrary input signal level higher than the power supply voltage to a reference logic level controlled by the power supply voltage quickly, reliably, and accurately. When a signal input to port A changes from the low level to the high level, the potential at node S_1 is immediately increased to a potential significantly higher than the power supply voltage due to the capacitive coupling of the drain-gate capacitance of NMOS transistor 10, so that NMOS transistor 14 turns on at bias circuit 12 in order to allow current to flow from node S_1 to power supply voltage terminal C, and the potential of node S_1 is clamped to level ($V_{CC} + V_{TN14}$), that is, above power supply voltage V_{CC} by threshold voltage V_{TN14}. As a result, a high level equal to the level below gate potential ($V_{CC} + V_{TN14}$) by threshold voltage V_{TN10}, that is, the potential of V_{CC}, is obtained at source of NMOS transistor 10, that is, port B.